Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Please cancel claims 23-27 without prejudice and amend claims 1, 3-7, 9, 12-15, and 17-22 as follows:

1. (currently amended) A processor with an instruction class controllable pipeline comprising:

a program storage unit holding a diverse plurality of class one and class two executable function instructions, the class one instructions having a ~~shorter~~ first execution latency and the class two instructions having a ~~longer~~ second execution latency, wherein the first execution latency is shorter than the second execution latency;

a fetch stage for fetching an instruction from the program storage unit to be stored in an instruction register;

a decode stage for classifying and decoding the instruction stored in the instruction register and generating an instruction class indication and storing decoded instructions in a decode register;

an adaptable pipeline control unit responsive to the instruction class indication for adapting the ~~pipeline to~~ latency of a pipeline stage dependent on the instruction class; and

an adaptable execution stage for execution of a decoded instruction stored in the decode register, the decoded instruction being a class one instruction or a class two instruction.

2. (original) The processor of claim 1, wherein the fetch stage further comprises:

a program counter and an instruction memory fetch mechanism which are operable to begin instruction processing by fetching one or more instructions from the program storage unit.

3. (currently amended) The processor of claim 1, wherein the executable function instructions comprise:

additions, subtractions, multiplications, divisions, compares, ANDs, ORs, ExclusiveORs, NOTs, shifts, rotates, permutes, bit operations, moves, loads, stores, communications ~~and variations and~~or combinations thereof.

4. (currently amended) The processor of claim 1, wherein the adaptable pipeline control unit further comprises:

a pipeline control mechanism for class one instructions to execute in ~~a~~ instructions having the first ~~time period~~ execution latency; and

a pipeline control mechanism for class two instructions to execute in ~~a~~ instructions having the second ~~longer time period~~ execution latency.

5. (currently amended) The processor of claim 4 wherein the pipeline control mechanism for class one instructions further comprises:

control for normal pipeline ~~sequencing~~ timing for class one instructions, ~~to execute in~~ wherein each stage of the normal pipeline has a duration equal to the ~~a~~ first ~~time period~~execution latency.

6. (currently amended) The processor of claim 4 wherein the pipeline control mechanism for class two instructions further comprises:

an instruction register feedback multiplexer;

a decode register feedback multiplexer;

a program counter and program counter update function;

a hold instruction register signal to control the instruction register feedback multiplexer to hold the contents of the instruction register for ~~a~~ the second ~~longer time period~~ execution latency upon detection of a class two instruction;

a hold decode register signal to control the decode register feedback multiplexer to hold the contents of the decode register for ~~a~~ the second ~~longer time period~~ execution latency upon detection of a class two instruction;

a hold program counter signal to control the program counter update function to hold the contents of the program counter for ~~a~~ the second ~~longer time period~~ execution latency upon detection of a class two instruction; and

a control for ~~extending pipeline sequencing~~the adaptable execution stage for the class two ~~instruction~~ instructions to execute ~~in a~~ instructions having the second ~~longer time period~~execution latency.

7. (currently amended) The processor of claim 4 wherein the pipeline control mechanism for class two instructions further comprises:

an instruction register gated clock;

a decode register gated clock;

a program counter gated clock;

instruction register clock gating logic responsive to the instruction class indication to extend the instruction register gated clock period for ~~a~~ the second ~~longer time period~~ execution latency upon detection of a class two instruction;

decode register clock gating logic responsive to the instruction class indication to extend the decode register gated clock period for ~~a~~ the second ~~longer time period~~ execution latency upon detection of a class two instruction;

program counter clock gating logic responsive to the instruction class indication to extend the program counter gated clock period for ~~a~~ the second ~~longer time period~~ execution latency upon detection of a class two instruction; and

control for ~~extending pipeline sequencing~~the adaptable execution stage for the class two instructions to execute ~~in a~~ instructions having the second ~~longer time period~~ execution latency.

8. (original) The processor of claim 7 wherein the instruction register gated clock, the decode register gated clock, and the program counter gated clock are a single gated clock.

9. (currently amended) The processor of claim 1 wherein the adaptable execution stage further comprises:

a class one execution unit operable to execute a class one instruction stored in the decode register, wherein the class one execution unit has the first execution latency; and

a class two execution unit operable to execute a class two instruction stored in the decode register, wherein the class two execution unit has the second execution latency.

10. (original) The processor of claim 1 wherein the decode stage further operates to decode an opcode field to classify an instruction.

11. (original) The processor of claim 1 wherein the decode stage further operates to decode an opcode field and decode of a data type field to classify an instruction.

12. (currently amended) The processor of claim 4 wherein the adaptable pipeline control unit further comprises:

a programmable clock gating mode indicator that specifies a normal clock gating mode and a slow down clock gating mode; and

control for extending pipeline ~~sequencing~~ stage timing both class 1 instructions and class 2 instructions to execute in a ~~third~~ longer time period than the second execution latency when the programmable clock gating mode indicator specifies a slow down clock gating mode.

13. (currently amended) A method for processor performance and power optimization of an instruction class adaptable pipeline processor supporting at least two classes of instructions with a first class operable ~~at a high frequency~~with a first latency for each pipeline stage of the adaptable pipeline and a second class operable ~~at a lower frequency~~with a second latency for each pipeline stage and where, the first latency is shorter than the second latency and where the instructions operable ~~at a higher frequency class~~ with the first latency can be specified to operate ~~at the higher frequency~~with the first latency ~~and~~ or the ~~lower frequency~~second latency and where the instructions operable ~~at the lower frequency~~with the second latency can be specified to ~~only~~ operate ~~at the lower frequency~~with the second latency ~~class~~, the method comprising:

programming the instruction class adaptable pipeline processor creating an application program containing a mix of two classes of instructions to meet functional requirements with ~~all~~ a first plurality of instructions used in the program operable ~~at the high frequency class~~ with the first latency specified in a format of each of the first plurality of instructions as class 1 instructions and with a second plurality of instructions used in the program operable with the second latency specified in a format of each of the second plurality of instructions as class 2 instructions; ~~and~~

modifying the application program ~~to meet performance and power requirements of an application~~ by changing, where appropriate, the format of class 1 instructions to class 2 instructions[[.]] to minimize power use while still meeting performance requirements of the application program; and

executing the application program on the instruction class adaptable pipeline processor.

14. (currently amended) A method for processor performance and power optimization of claim 13 ~~wherein modifying the application program to meet performance and power requirements of an application, the method~~ further comprises:

appropriately programming a programmable clock gating mode to cause a specifiable majority of the instructions of the class adaptable pipeline processor to execute at a ~~lower clock frequency~~ longer latency than the second latency associated with the class 2 ~~clock frequency~~ instructions, to further minimize power use while still meeting performance

requirements of the application program~~to meet performance and power requirements of an application~~.

15. (currently amended) A very long instruction word (VLIW) processor with a plurality of instruction class controllable pipelines comprising:

a VLIW storage unit holding a diverse plurality of class one and class two executable function instructions located in multiple instruction slot format VLIWs, the class one instructions having a ~~shorter~~ first execution latency and the class two instructions having a longer second execution latency;

a VLIW fetch stage for fetching a VLIW from a VLIW storage unit to be stored in a VLIW instruction register (VIR);

a decode stage for classifying and decoding the plurality of executable function instructions stored in the VIR, and generating an instruction class indication for each of the plurality of executable function instructions and storing decoded instructions in a plurality of instruction slot specific decode registers;

an adaptable pipeline control unit responsive to the instruction class indications from the classified plurality of executable function instructions for adapting the ~~pipeline~~ latency of each stage of the plurality of instruction class controllable pipelines dependent on ~~to~~ the instruction class indications; and

a plurality of adaptable execution stages each operable for execution of a decoded instruction stored in an instruction slot specific decode register, the decoded instruction being a class one instruction or a class two instruction.

16. (original) The VLIW processor of claim 15, wherein the VLIW fetch stage further comprises:

a VLIW memory control unit which is operable to begin VLIW processing by fetching a VLIW from the VLIW storage unit.

17. (currently amended) The processor of claim 15, wherein the executable function instructions comprise:

additions, subtractions, multiplications, divisions, compares, ANDs, ORs, ExclusiveORs, NOTs, shifts, rotates, permutes, bit operations, moves, loads, stores, communications ~~and variations and~~or combinations thereof;

18. (currently amended) The processor of claim 15, wherein the adaptable pipeline control unit further comprises:

a pipeline control mechanism for a VLIW, the VLIW consisting of all class one instructions, to control the execution of the VLIW with ~~execute in a~~ the first ~~time period~~ execution latency; and

a pipeline control mechanism for a VLIW, the VLIW consisting of at least one class two instruction, to control the execution of the VLIW with ~~execute in a~~ the second ~~longer time period~~ execution latency.

19. (currently amended) The processor of claim 18 wherein the pipeline control mechanism for a VLIW consisting of all class one instructions further comprises:

control for normal pipeline ~~sequencing~~ timing for the class one instructions ~~to execute in a~~, wherein each stage of the normal pipeline has a duration equal to the first ~~time period~~execution latency.

20. (currently amended) The processor of claim 18 wherein the pipeline control mechanism for a VLIW consisting of at least one class two instruction further comprises:

VIR state maintaining multiplexers;

decode register state maintaining multiplexers;

a program counter and program counter update function;

a hold VIR signal to control the VIR state maintaining multiplexers to hold the contents of the VIR for ~~a~~ the second ~~longer time period~~ execution latency upon detection of the at least one class two instruction;

a plurality of hold decode register signals to control the decode register state maintaining multiplexers to hold the contents of the decode registers for ~~a~~ the second ~~longer time period~~ execution latency upon detection of the at least one class two instruction;

a hold program counter signal to control the program counter update function to hold the contents of the program counter for ~~a~~ the second ~~longer time period~~ execution latency upon detection of the at least one class two instruction; and

control for ~~extending pipeline sequencing~~ the plurality of adaptable execution stages ~~for the VLIW~~ to execute the VLIW ~~in~~with ~~a~~ the second ~~longer time period~~ execution latency.

21. (currently amended) The processor of claim 18 wherein the pipeline control mechanism for a VLIW consisting of at least one class two instruction further comprises:

a VIR gated clock;

a plurality of decode register gated clocks;

a program counter gated clock;

VIR clock gating logic responsive to the plurality of instruction class indications to extend the VIR gated clock period for ~~a~~ the second ~~longer time period~~execution latency upon detection of the at least one class two instruction;

a plurality of decode register clock gating logic responsive to the plurality of instruction class indications to extend the decode register gated ~~clocks~~ clock period for ~~a~~ the second ~~longer time period~~ execution latency upon detection of the at least one class two instruction;

program counter clock gating logic responsive to the plurality of instruction class indications to extend the program counter gated clock period for ~~a~~ the second ~~longer time period~~ execution latency upon detection of the at least one class two instruction; and

control for ~~extending pipeline sequencing~~the plurality of adaptable execution stages ~~for the VLIW~~ to execute the VLIW ~~in~~with ~~a~~ the second ~~longer time period~~ execution latency.

22. (currently amended) The processor of claim 15 wherein each adaptable execution stage of the plurality of adaptable execution stages further comprises:

a class one execution unit operable to execute a class one instruction stored in the decode register, wherein the class one execution unit has the first execution latency; and

a class two execution unit operable to execute a class two instruction stored in the decode register, wherein the class two execution unit has the second execution latency.

23-27 (canceled)